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Hiroshi ITAHARA.
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For: Synchronous Follow-up Apparatus and Synchronous Follow-up Method
Assistant Commissioner for Patents
Alexandria, VA 22313-1450

STATEMENT UNDER 37 C.F.R. 1.55(a)

Sir,

I, Tomonori Nakamura, hereby declare that I am conversant with both English and Japanese languages, and certify to best of my knowledge and belief that the attached are true and correct English translation of Japanese Patent Application No. 2004-10612 filed on July 19, 2004.

T. Nakamura

Tomonori Nakamura

Date: April 4, 2008

Patent Office

Japanese Government

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[List of Filed Documents]

[Filed Document Name] Specification 1

[Filed Document Name] Drawing 1

[Filed Document Name] Abstract 1

[Number of General Power] 0002926

[Designation of Document] Claims

[Claim 1] A synchronous follow-up apparatus comprising:

a PLL portion which has a voltage controlled oscillating portion and a control voltage generating portion for carrying out a phase comparison to compare phase of a receiving signal and a signal output from the voltage controlled oscillating portion with each other, thereby detecting a phase difference, and for generating a control voltage signal to be input to the voltage controlled oscillating portion based on the phase difference thus detected, and outputs the signal output from the voltage controlled oscillating portion as a first clock signal; and

a control loop portion having a reference frequency signal generating portion, a second clock signal generating portion for generating a signal having the same frequency as a frequency of the first clock signal from the reference frequency signal generating portion, and a frequency control signal generating portion for generating a frequency control signal to change the frequency of the second clock signal generating portion and outputting the frequency control signal to the second clock signal generating portion based on a difference in a frequency after a predetermined time between the first clock signal and the second clock signal.

[Claim 2] The synchronous follow-up apparatus according to claim 1, wherein the frequency control signal generating portion outputs a frequency control signal which is successfully subjected to frequency tuning in the closest past when an error having a predetermined value or more is detected between the frequency of the first clock signal and that of the second clock signal, and the second clock signal generating portion outputs, as a radio reference signal, the second clock signal generated based on the frequency control signal.

[Designation of Document] Specification
[Title of the Invention] Synchronous Follow-Up Apparatus
[Technical Field]
[0001]
The present invention relates to a synchronous follow-up apparatus.
[Background Art]
[0002]
There has been a CPRI (Common Public Radio Interface) (registered trademark) as the standard of an interface between a radio equipment control (REC) for carrying out a baseband processing and a radio equipment (RE) for carrying out a radio signal processing in the case in which the internal structure of a base station apparatus such as a WCDMA mobile telecommunication system is divided into the radio equipment control and the radio equipment and they are connected to each other through a digital transmission path (see Non-Patent Document 1).
[0003]
Fig. 7 is a diagram showing a relationship between the radio equipment control and the radio equipment. A base station apparatus 200 is constituted to have a radio equipment control 201 and a radio equipment 202, and the radio equipment control 201 and the radio equipment 202 are connected to each other through a digital transmission path 203 for transmitting an electric signal or a light signal.
[0004]
The radio equipment control 201 is connected to a radio network control (RNC) 210 to carry out the baseband processing. Moreover, the radio equipment 202 serves to carry out a processing in a radio frequency band and to perform a radio communication with a terminal device 220.
[0005]
In the standard of the CPRI (registered trademark), a line rate in the digital transmission path 203 is defined, and the reference frequency of the radio equipment 202 is to be

synchronized with the reference frequency of the line rate. In the standard of the CPRI, there are 32 basic demand items. Above all, there are the following three demand items for a synchronizing performance.

[0006]

A first demand is that an fc (line selection lock frequency) synchronizing range of 300 Hz in the radio equipment is to be ensured (a demand number of R-17), a second demand is that a jitter stability in the radio equipment (an REC-RE synchronizing system after a synchronization) is to be ensured at ±0.002 ppm (R-18), and a third demand is that a synchronization is to be established in a line clock OFF-ON transient state within 10 seconds (R-30).

[0007]

However, these three demands are contrary to each other in the case in which a synchronizing loop is to be designed by using an ordinary PLL circuit. For example, when the PLL circuit is designed in order to ensure a lock range demanded in the R-17, it is impossible to ensure a precision in a synchronization which is demanded in the R-18. In order to ensure the precision in the synchronization which is demanded in the R-18, furthermore, it is very hard to establish the synchronization in a time demanded in the R-30. Accordingly, there is a situation in which it is very hard to satisfy these demands at the same time.

[Non-Patent Document 1] "CPRI Specification", First Edition, September 30, 2003

[Disclosure of the Invention]

[Problems that the Invention is to Solve]

[0008]

In consideration of the circumstances, it is an object of the invention to provide a synchronous follow-up apparatus capable of implementing a synchronization establishing time having a high precision in a synchronization within a constant time while ensuring a lock range.

[Means for Solving the Problems]

[0009]

The invention provides a synchronous follow-up apparatus comprising a PLL portion which has a voltage controlled oscillating portion and a control voltage generating portion for carrying out a phase comparison to compare phase of a receiving signal and a signal output from the voltage controlled oscillating portion with each other, thereby detecting a phase difference, and for generating a control voltage signal to be input to the voltage controlled oscillating portion based on the phase difference thus detected, and outputs the signal output from the voltage controlled oscillating portion as a first clock signal, and a control loop portion having a reference frequency signal generating portion, a second clock signal generating portion for generating a signal having the same frequency as a frequency of the first clock signal from the reference frequency signal generating portion, and a frequency control signal generating portion for generating a frequency control signal to change the frequency of the second clock signal generating portion and outputting the frequency control signal to the second clock signal generating portion based on a difference in a frequency after a predetermined time between the first clock signal and the second clock signal.

[0010]

By the structure, it is possible to implement a synchronization establishing time having a high precision in a synchronization within a constant time while ensuring a lock range by the PLL portion for maintaining the lock range and the control loop portion for ensuring a high precision in a synchronization and implementing a short synchronization establishing time.

[0011]

Moreover, the frequency control signal generating portion outputs a frequency control signal which is successfully subjected to frequency tuning in the closest past when an error having a predetermined value or more is detected between the frequency of the first clock signal and that of the second clock signal, and the second clock signal generating portion outputs,

as a radio reference signal, the second clock signal generated based on the frequency control signal.

[0012]

By the structure, also in the case in which a fault is caused on a receiving signal for some reason, a stable radio reference signal can be output within the range of the reference frequency accuracy of the reference signal generating portion.

[Advantage of the Invention]

[0013]

According to the invention, it is possible to provide a synchronous follow-up apparatus capable of implementing a synchronization establishing time having a high precision in a synchronization within a constant time while ensuring a lock range.

[Best Mode for Carrying Out the Invention]

[0014]

Prior to an embodiment of the invention, the synchronous follow-up of a CPRI (registered trademark) interface will be investigated in respect of the case in which a synchronizing loop using a PLL is to be implemented. In the CPRI (registered trademark), there are defined three types of line rates of the transmission path for connecting the radio equipment control and the radio equipment which have been described in the Background Art. In the following, description will be given to the case in which the line rate of a digital transmission path is 1228.8 [Mbps] to be one of the defined line rates.

[0015]

Fig. 6 is a diagram showing an example of a structure in which a synchronizing loop using a PLL is utilized for the CPRI (registered trademark) interface. As shown in Fig. 6, the interface comprises a serializer/deserializer (which will be hereinafter referred to as a SERDES) synchronizing loop having a SERDES 10 connected to a digital transmission path 220, a jitter remover 20 of a PLL base and a voltage controlled crystal oscillator (hereinafter referred to as a VCXO) 30, and an interface portion 140 for inputting, as a line clock, a clock

signal output from the VCXO 30.

[0016]

The SERDES 10 serial/parallel converts a serial signal received through the transmission path 220 into a parallel signal and transmits the received data to the interface portion 140, and regenerates and outputs a receiving clock signal (RXCLK). The jitter remover 20 has a PLL base, and sets the receiving clock signal output from the SERDES 10 to be a reference signal (REF) and carries out a phase comparison with a signal (VCO) input from the VCXO 30, and converts the same signal into a voltage signal to be output as a control voltage (CP) of the VCXO 30. Thus, a PLL is constituted by the jitter remover 20 and the VCXO 30.

[0017]

A signal output from the VCXO 30 is input as a transmission clock (TXCLK) of the SERDES 10, and furthermore, is input as a line clock (LINECLK) of the interface portion 140.

[0018]

The lock range of the PLL constituted by the jitter remover 20 and the VCXO 30 is to be set to 300 Hz (0.1 ppm) in accordance with the demand item R-17. In order to cover the lock range, however, it is impossible to regulate the loop bandwidth and loop gain of the PLL in order to ensure a precision in a synchronization of $\pm$0.002 ppm which is demanded in the R-18. To the contrary, in the case in which the regulation is carried out in order to ensure the precision in a synchronization which is demanded in the R-18, it is impossible to cover the lock range demanded in the R-17.

[0019]

Furthermore, the signal output from the VCXO which has the output frequency of the PLL is input as the line clock of the interface portion. In the CPRI (registered trademark), however, the line clock is also used as a reference signal for a radio signal processing. Accordingly, an excellent CN characteristic is also demanded.

[0020]

If the precision in a synchronization which is demanded in the R-18 is to be ensured, it is hard to implement the provisions of the R-30. The PLL regulated to ensure the precision in a synchronization gives a transient response slowly. For this reason, in the case in which a precision of ±0.002 ppm demanded in the R-18 is to be ensured, it is really impossible to carry out lock-up within 10 seconds which is demanded in the R-30.

[0021]

In consideration of the investigations, a control loop for ensuring a high precision in a synchronization and implementing a short synchronization establishing time is provided in addition to the PLL for maintaining a lock range. Consequently, it is possible to implement a synchronous follow-up apparatus which satisfies the demands of the CPRI (registered trademark), for example.

[0022]

An embodiment of the invention will be described below with reference to the drawings. Fig. 1 is a diagram showing the schematic structure of a synchronous follow-up apparatus according to the embodiment of the invention. Overlapping portions with the portions in Fig. 6 have the same reference numerals.

[0023]

As shown in Fig. 1, the synchronous follow-up apparatus according to the embodiment comprises a SERDES 10 connected to a digital transmission path 220, a jitter remover 20, a VCXO 30, an interface portion 40, a direct digital synthesizer 50, and a temperature controlled crystal oscillator (hereinafter referred to as an OCXO) 60.

[0024]

The jitter remover 20 and the VCXO 30 constitute a PLL for setting, as a reference signal, a receiving clock signal output from the SERDES 10 as described with reference to Fig. 6. The jitter remover 20 and the VCXO 30 are designed to satisfy a lock range of 300 Hz which is demanded in the R-17. In demand items R-27 and R-28, furthermore, it is demanded that a bit error

rate (BER) in a data transmission is to be equal to or less than 10^{-12}. The design is also carried out in order to satisfy this demand. Consequently, it is possible to ensure the quality of the transmission of a digital transmission line.

[0025]

The DDS 50 creates, from a reference signal sent from the OCXO 60, a local clock signal (LOCALCLK) having the same frequency as the frequency of a line clock signal to be regenerated from the digital transmission path and output from the PLL, and inputs the local clock signal to a calculating circuit 41 of the interface portion 40. The calculating circuit 41 generates a frequency control signal (FSW) based on a difference in a frequency after a predetermined time which is made between the input line clock signal and local clock signal, and outputs the frequency control signal to the DDS 50.

[0026]

The DDS 50 corrects the local clock signal based on the frequency control signal sent from the calculating portion 41. Thus, it is possible to satisfy a demand for a synchronization establishing time while ensuring a precision in a synchronization through a control loop formed by the line clock signal, the frequency control signal and the local clock signal.

[0027]

The control loop will be described below in detail. Fig. 2 is a diagram showing a control loop including the schematic structure of the calculating portion. A normal line clock signal has a standard value of approximately 1/16 to 1/20 minute of a line rate (1.2288 GHz in the embodiment), that is, 76.8 MHz to 61.44 MHz. In the embodiment, description will be given by taking, as an example, the case in which the line clock signal has a frequency of 61.44 MHz.

[0028]

As shown in Fig. 2, the calculating portion 41 has a first counter 411, a second counter 412, an adder 413 and an FSW calculator 414.

[0029]

The first counter 411 is operated synchronously with the frequency of the line clock signal which is input.

Moreover, the second counter 412 is operated synchronously with the frequency of the local clock signal sent from the DDS 50. A difference after a predetermined time between the first counter 411 and the second counter 412 is observed as a phase difference M between two clock signals. The FSW calculator 414 generates the frequency control signal of the DDS 50 based on the phase difference M.

[0030]

For example, in the case in which the counter phase difference M is detected as a phase difference after Z seconds, it is given by Equation (1).

$$M = Y \cdot Z - X \cdot Z \quad \cdots \quad (1)$$

[0031]

Herein, Y represents a frequency [Hz] of a local clock signal, X represents a frequency [Hz] of a line clock signal, and Z represents a counter observing time [second].

[0032]

The line clock signal is synchronized with data transmitted from a radio equipment control 201. For this reason, a reference precision is set to be ± 0.05 ppm in accordance with a 3GPP standard, for example. Since the local clock signal is synchronized with a reference precision (for example, ± 0.1 ppm) from the OCXO 60, a precision of ± 0.1 ppm is obtained.

[0033]

Based on the Equation (1), a frequency difference (Y - X) between the local clock signal and the line clock signal is given by Equation (2).

$$(Y - X) = M/Z \ [Hz] \quad \cdots \quad (2)$$

[0034]

Assuming that the frequency X of the line clock signal is 61.44 [MHz], a tuning frequency Y is given by Equation (3).

$$Y = 61.44 \times 10^6 + M/Z \ [Hz] \quad \cdots \quad (3)$$

[0035]

Then, a control is carried out to change the frequency

of the DDS 50 based on the tuning frequency Y.

A frequency tuning word (FSW) to be a frequency control signal has a value obtained by dividing the tuning frequency by a minimum resolution frequency Δf of the DDS 50 as shown in Equation (4).

$$FSW = \text{tuning frequency } Y / \Delta f \quad \cdots \quad (4)$$

[0036]

Usually, the DDS 50 has a frequency resolution which is a fraction of the power of two (R : approximately 32, ordinarily) of a sampling rate. In the embodiment, the frequency of the OCXO 60 is set to be 10 MHz and the sampling rate of the DDS 50 is set to be 200 MHz which is twenty times as great as that of the OCXO 60. If R = 32 is set, a frequency correcting resolution per FSW1 unit is $200 \times 10^6 / 2^{32} = 0.046$ [Hz].

[0037]

The frequency correcting resolution ensures a precision of 0.00075 ppm for a comparison frequency of 61.44 MHz. In order to achieve a synchronizing precision of 0.002 ppm, a count observing time of 8.2 seconds is theoretically required when a comparison frequency of 61.44 MHz is used.

[0038]

Fig. 3 is a chart showing a tuning convergence characteristic. In Fig. 3, a curve 301 represents a simulation result of a tuning convergence characteristic on a line clock signal from a line clock signal (+0.005 ppm) and a local clock signal (-0.1 ppm), and a curve 302 represents a simulation result of a synchronizing convergence characteristic on a line clock signal from a line clock signal (-0.005 ppm) and a local clock signal (+0.1 ppm). As shown in Fig. 3, it is apparent that a synchronizing precision of 0.002 ppm is achieved in an observing time after a theoretical value of approximately 8.2 seconds. Thus, the synchronizing precision of 0.002 ppm demanded in the R-18 can satisfy a synchronizing establishment within 10 seconds which is demanded in the R-30.

[0039]

Thus, the control loop for ensuring a high precision in

a synchronization and implementing a short synchronization establishing time is provided in addition to the PLL for maintaining a lock range. Consequently, it is possible to implement a synchronization establishing time having a high precision in a synchronization within a constant time while ensuring the lock range.

[0040]

Next, description will be given to a control for the cutoff, disturbance and instantaneous stop of a line clock signal which is caused by the fault of a digital transmission path. Fig. 4 is a diagram showing the operation of the FSW calculator in the fault of the line clock.

[0041]

As shown in Fig. 4, the FSW calculator 414 first acquires a phase difference M (Step S401). Then, a tuning frequency and a line clock frequency are compared with each other based on the phase difference M thus acquired (Step S402). If an error between these frequencies has a predetermined value (0.15 ppm in the embodiment) or less, FSW is set to be FSW' (Step S403). At this time, the FSW is set (Step S404). The FSW' represents FSW which is successfully subjected to frequency tuning in the closest past. The predetermined value of the error, that is, 0.15 ppm is a maximum error between the maximum difference (±0.1 ppm) of the OCXO and the frequency precision difference of the reference frequency (±0.05 ppm) of the radio equipment control (RES).

[0042]

If the error between these frequencies is greater than the predetermined value (0.15 ppm in the embodiment), the FSW' to be the FSW subjected to tuning in the closest past is substituted for the FSW (S404) and is set to be the FSW (Step S405).

[0043]

More specifically, in this example, it is decided whether or not a fault is generated on the line clock depending on the difference between the tuning frequency and the line clock frequency. If it is decided that the fault is generated, the

frequency of the DDS is controlled by using a frequency control signal which is successfully subjected to the frequency tuning in the closest past.

[0044]

The DDS 50 sets the OCXO 60 to have a reference frequency. Therefore, it is possible to ensure the stability of a reference signal for a radio processing within the stability of the OCXO 60 (for example, ±0.1 ppm). Also in the case in which a fault is generated on the line clock for some reason, for example, the disconnection of the digital transmission path, accordingly, it is possible to ensure the stability of the output radio frequency of the radio equipment 202.

[0045]

Moreover, the CN characteristic of an RF reference signal can also be ensured to be high by the OCXO 60 and the DDS 50 irrespective of the quality of the line clock signal. Therefore, it is possible to obtain the stability by causing an EVM (Error Vector Magnitude) or a PCDE (Peak Code Domain Error) to be independent of the quality of the transmission of the line clock signal.

[0046]

By such a structure, it is possible to implement a synchronizing performance which is demanded, and furthermore, to obtain the absolutely stable and excellent CN characteristic of an RF reference signal within the range of the reference frequency accuracy of the OCXO, thereby enhancing the radio performance of the radio equipment (RE).

[0047]

Fig. 5 is a diagram showing another example of the synchronous follow-up apparatus according to the embodiment of the invention. In this example, there is shown the case in which an LSI having a PLL function and a sufficient lock performance (for example, approximately ±10 ppm) is used as a SERDES 70. By using the SERDES 70, it is possible to eliminate the jitter remover shown in Fig. 1, thereby simplifying the structure of the synchronous follow-up apparatus.

[Industrial Applicability]

[0048]

The synchronous follow-up apparatus according to the invention has an advantage that it is possible to implement a synchronous establishing time having a high precision in a synchronization within a constant time while ensuring a lock range, and is useful for a radio equipment in a base station apparatus in the CPRI (registered trademark).

[Brief Description of the Drawings]

[0049]

Fig. 1 is a diagram showing the schematic structure of a synchronous follow-up apparatus according to an embodiment of the invention,

Fig. 2 is a diagram showing a control loop including the schematic structure of a calculating portion,

Fig. 3 is a chart showing a tuning convergence characteristic,

Fig. 4 is a diagram showing the operation of an FSW calculator in the fault of a line clock,

Fig. 5 is a diagram showing another example of the synchronous follow-up apparatus according to the embodiment of the invention,

Fig. 6 is a diagram showing an example of a structure in the case in which a synchronous loop using a PLL is utilized, and

Fig. 7 is a diagram showing a relationship between a radio equipment control and a radio equipment.

[Description of the Reference Numerals and Signs]

[0050]

10, 70	SERDES
20	jitter remover
30	VCXO
40	interface portion
41	calculating portion
50	DDS
60	OCXO

411, 412	counter
413	adder
414	FSW calculator
200	base station apparatus
201	radio equipment control
202	radio equipment
203	digital transmission path

[Designation of Document] Abstract

[Abstract]

[Problem] It is an object to provide a synchronous follow-up apparatus capable of implementing a synchronization establishing time having a high precision in a synchronization within a constant time while ensuring a lock range.

[Means for Resolution] A line clock signal is generated to ensure a lock range by a PLL having a voltage controlled oscillating portion 50, and a jitter remover 20 for carrying out a phase comparison to compare phases of a receiving clock signal regenerated by a SERDES 10 and a signal output from the voltage controlled oscillating portion 50, thereby detecting a phase difference, and generating a control voltage signal to be input to the voltage controlled oscillating portion based on the phase difference thus detected. Moreover, a precision in a synchronization and a synchronization establishing time within a constant time are ensured by a control loop portion having an OCXO 60, a DDS 50 for generating, from the OCXO 60, a signal having the same frequency as the frequency of a line clock signal, and a calculating portion 41 for calculating a frequency control signal to change the frequency of the DDS 50 based on a difference in a frequency after a predetermined time between the line clock signal and a local clock signal.

[Selected Drawing] Fig. 1

Fig. 1

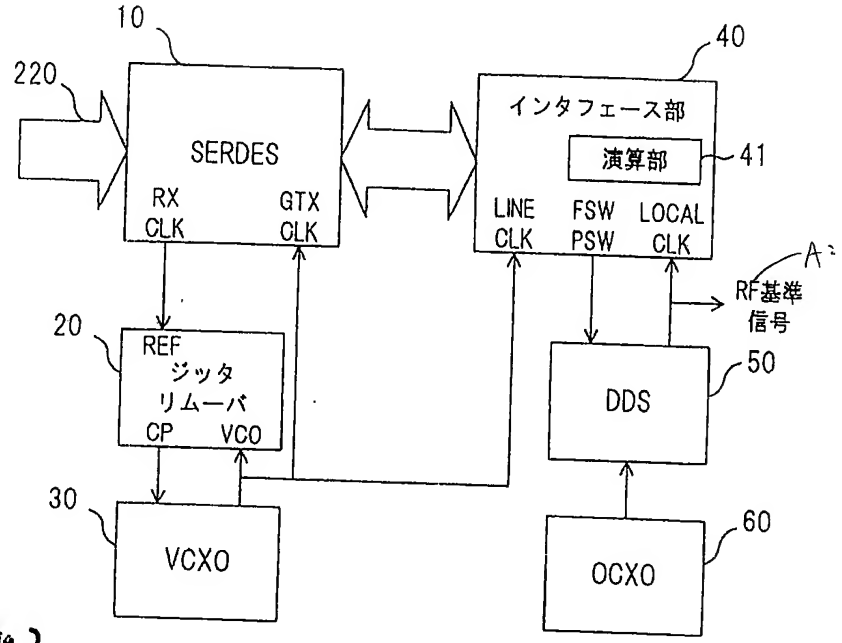

FIG. 1

20	JITTER REMOVER
40	INTERFACE PORTION
41	CALCULATING PORTION

A: RF REFERENCE SIGNAL

Fig. 2

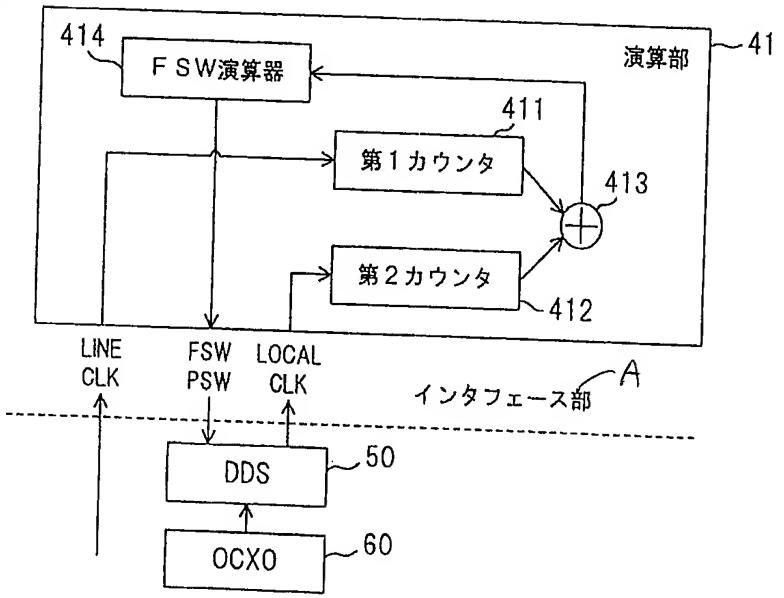

FIG. 2

41	CALCULATING PORTION
411	FIRST COUNTER
412	SECOND COUNTER
414	FSW CALCULATOR

A: INTERFACE PORTION

Fig. 3

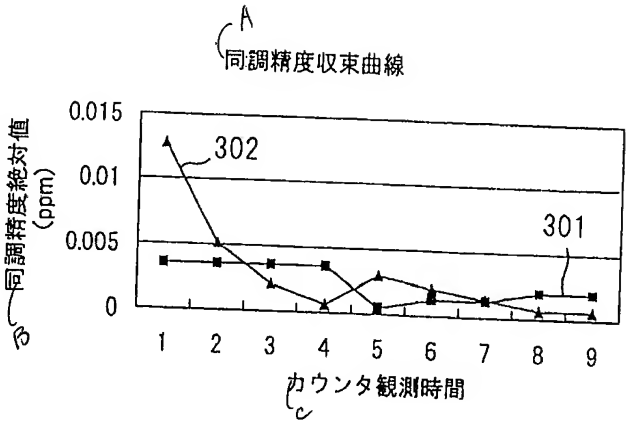

FIG. 3

A: TUNING PRECISION CONVERGENCE CURVE

B: TUNING PRECISION ABSOLUTE VALUE

C: COUNTER OBSERVING TIME

Fig. 4

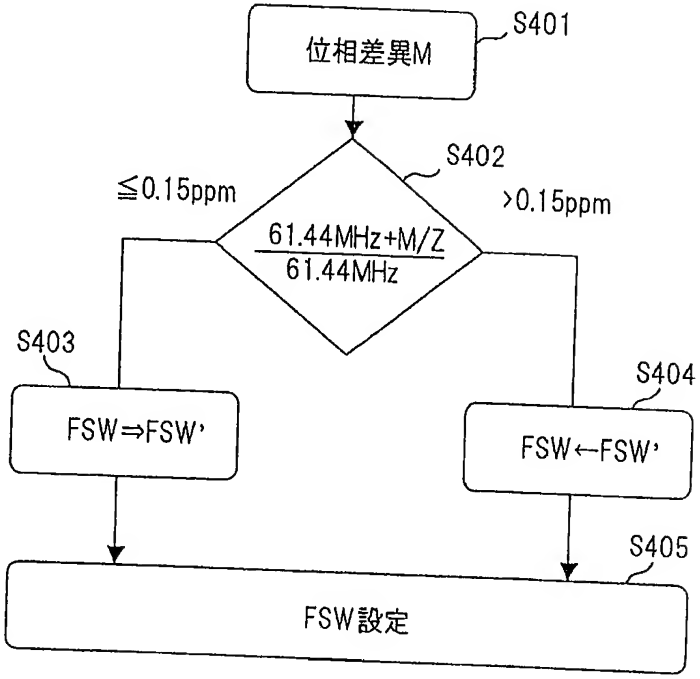

FIG. 4

S401 PHASE DIFFERENCE M

S405 SET FSW

Fig. 5

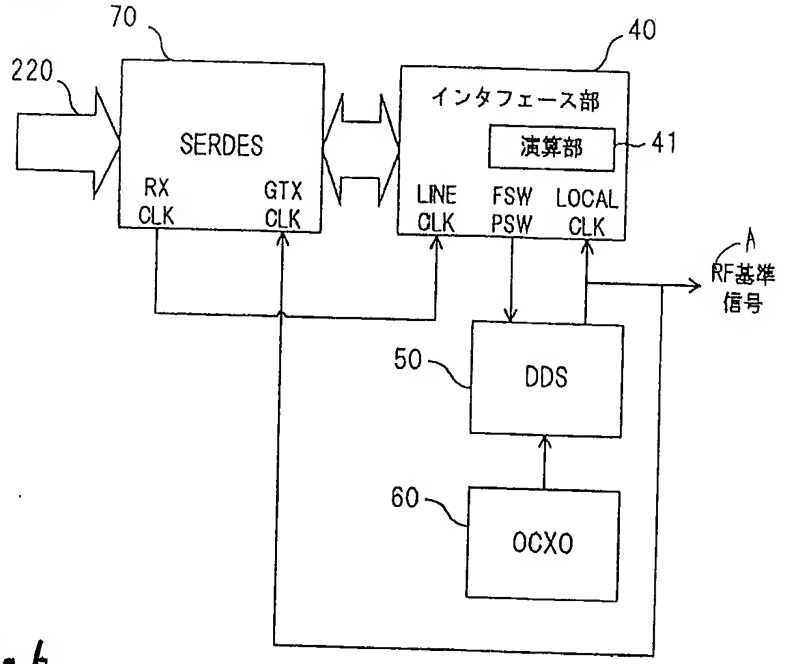

FIG. 5

40 INTERFACE PORTION

41 CALCULATING PORTION

A: RF REFERENCE SIGNAL

Fig. 6

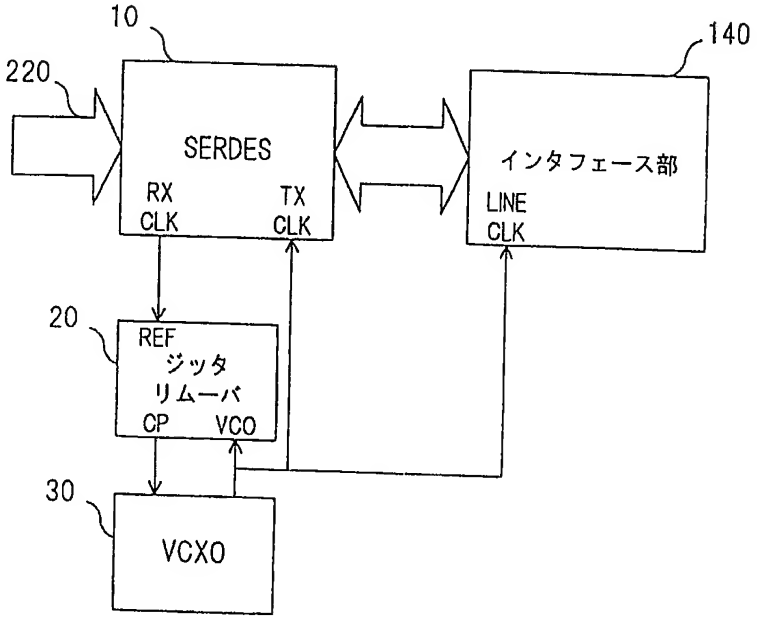

FIG. 6

20 JITTER REMOVER

140 INTERFACE PORTION

Fig. 7

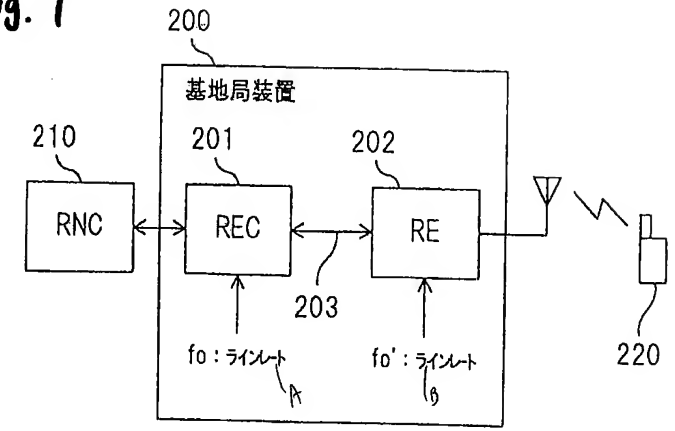

FIG. 7

200 BASE STATION APPARATUS

A: LINE RATE

B: LINE RATE